



Sheet 1 of 1

Form 1449*	Atty. Docket No.: 303.572US1	Serial No. 09/253,611
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Paul A. Farrar	
	Filing Date: February 19, 1999	Group: 2812

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
						If Appropriate
RP	3,959,047	05/25/1976	Alberts, G.S., et al.	156	8	09/30/74
RP	5,240,878	08/31/1993	Fitzsimmons, et al.	437	187	04/26/91
RP	5,457,345	10/10/1995	Cook, H.C., et al.	257	766	01/14/94
RP	5,461,257	10/24/1995	Hundt, M.J.	257	707	03/31/94
RP	5,642,261	06/24/1997	Bond, R.H., et al.	361	704	06/30/94
RP	5,693,572	12/02/1997	Bond, R.H., et al.	437	209	01/18/96

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

RP	Anonymous, "Combination Process for Final Metal Lines and Metal Terminals", Kenneth Mason Publications Ltd, Research Disclosure No. 342, England, 1, (Oct. 1992)
RP	Anonymous, "Process for High Density of Chip Terminals on Large Wafers", Kenneth Mason Publications Ltd, Research Disclosure No. 02, England, 1, (Feb. 1993)
RP	ASM International, "Packaging", ASM International Electrotronic Materials Handbook Vol. 1, 301 and 440p,
RP	Marcotte, V.C., et al., "Review of Flip Chip Bonding", Proceedings of the 2nd ASM International Electronic Materials and Processing Congress 24-28 April 1989, Philadelphia, PA, 73-81, (1989)
RP	Pfeiffer, L., et al., "Self-Aligned Controlled Collapse Chip Connect (SAC4)", Journal of the Electrochemical Society, Vol. 134, No. 11, 2940-2941, (Nov. 1987)
RP	Ryan, J.G., et al., "Technology Challenges for Advanced Interconnects", 1-5 p.,

Examiner

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*Substitute Disclosure Statement Form (PTO-1449)

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